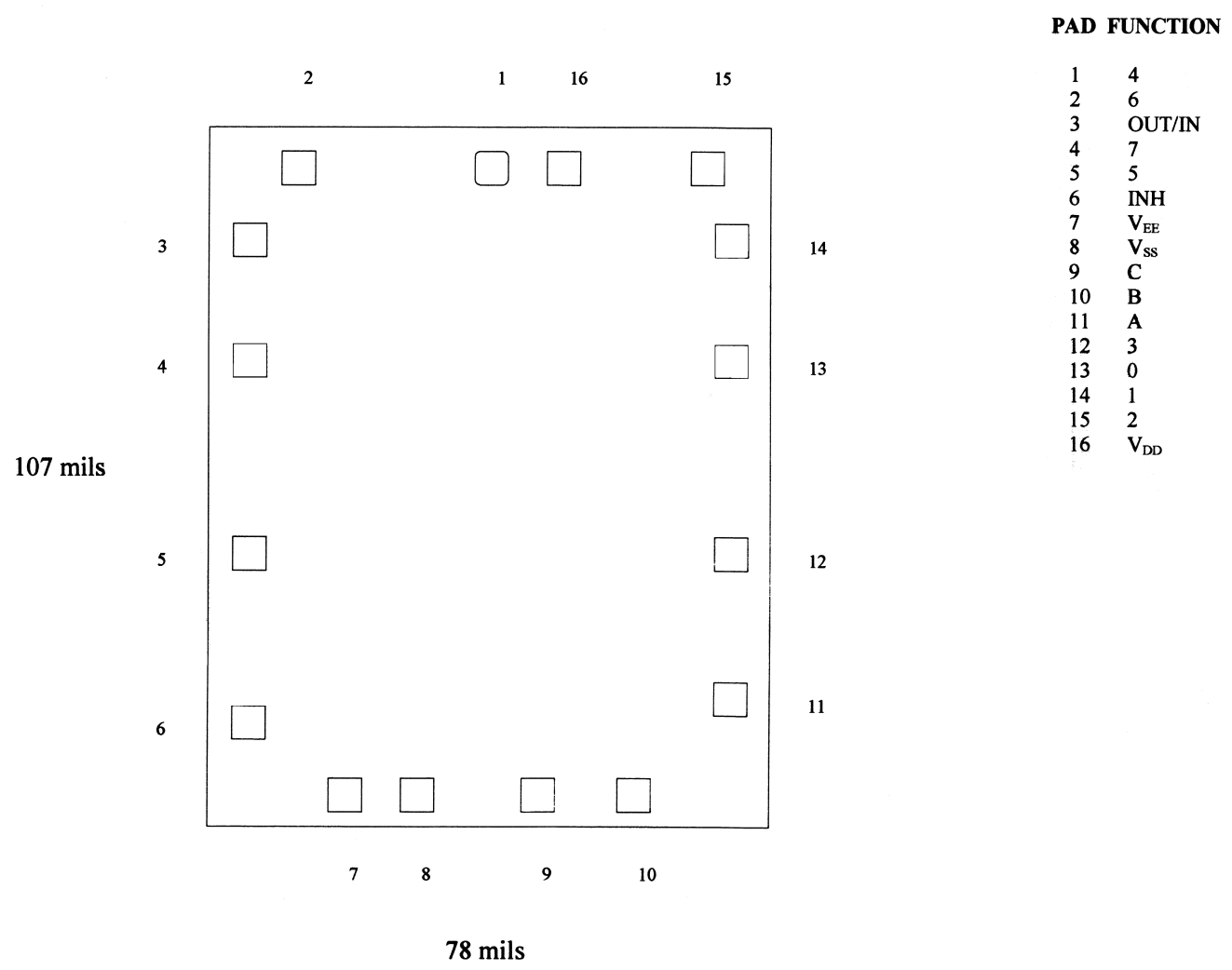
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material: Al**

**Backside Material: Si Ni**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VDD (or leave FLOATING)**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .078” X .107” DATE: 8/7/18**

**MFG: TEXAS INSTR. / HARRIS THICKNESS .024” P/N: CD4051B**

**DG 10.1.2**

#### Rev B, 7/19/02